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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/621,614	07/21/2000	Yasuyuki Morishita	040373/0287	4521

22428 7590 04/23/2004

FOLEY AND LARDNER  
SUITE 500  
3000 K STREET NW  
WASHINGTON, DC 20007

EXAMINER

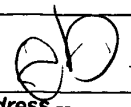
NADAV, ORI

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/621,614	<b>Applicant(s)</b> MORISHITA, YASUYUKI	
	<b>Examiner</b> ori nadav	<b>Art Unit</b> 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on 03 February 2004.

2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) 1-10 is/are pending in the application.

    4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.

6) ☒ Claim(s) 1-10 is/are rejected.

7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.

8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some    c) ☐ None of:  
         1. ☐ Certified copies of the priority documents have been received.  
         2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
         3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
     \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6) <input type="checkbox"/> Other: _____
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## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Duvvury et al. (5,814,865).

APA teaches in figure 7 a semiconductor device having, on a semiconductor substrate 20, an input/output protection circuit section comprising a complementary N type field effect transistor wherein the complementary field effect transistor includes a first field effect transistor having source 3c and drain 3b diffusion layers of the first conductive type, respectively, and a gate electrode 6 that is disposed between these source and drain diffusion layers of the first conductivity type, and a second field effect transistor having source 4c and drain 4b diffusion layers of the second conductive type, respectively, and a gate electrode 5 that is disposed between these source and drain diffusion layers of the second conductivity type, wherein a source dopant diffusion region 4a of the second conductive type is set at a distance from the first field effect transistor, and a drain dopant diffusion region 3a of the first conductive type is set at a distance from the second field effect transistor,

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an element isolation film 10 located in the substrate between the dopant diffusion region and the source diffusion layer of the first conductivity type for separating the dopant diffusion region from the source diffusion layer,

wherein the drain dopant diffusion region 4a is connected to a first reference potential  $V_{ss}$ , the drain dopant diffusion region 3a is connected to a second reference potential  $V_{dd}$ , and the drain diffusion layer 3b and the drain diffusion layer 4b of the first and second field effect transistors, respectively, are each connected directly to an input/output terminal section 7 without an intervening resistance element, and wherein the source diffusion layer of the first field effect transistor is connected to a constant ground terminal 9 and not connected to an input/output terminal section..

APA does not teach a first conductive type well formed directly under the first source diffusion layer and thereby the first conductive type well is electrically connected directly with the source diffusion layer, and at least partially underlies the element isolation film, and having a lower dopant concentration than the first diffusion layer.

Duvvury et al. teach in figure 2 and related text a first conductive type well 204 formed directly under the first source diffusion layer 212 and thereby the first conductive type well is electrically connected directly with the source diffusion layer, and underlies a dopant diffusion region of the second conductivity type 210, and having a lower dopant concentration than the first diffusion layer.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first conductive type well under the first diffusion layer, having a lower dopant concentration than the first diffusion layer in APA's device in

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order to provide better electrical isolation to the device by forming the transistor in an n-well.

Regarding the claimed limitation of a first conductive type well at least partially underlies the element isolation film, this feature is inherent in the device of APA and Duvvury et al., because the first conductive type well stretches between the first source diffusion layer and the dopant diffusion region of the second conductivity type. Since the element isolation film is located between the between the first source diffusion layer and the dopant diffusion region of the second conductivity type, then the first conductive type well at least partially underlies the element isolation film, as claimed.

Regarding claim 1, APA teaches in figures 14-15 and related text that an input/output protection circuit generally composed of a plurality of field effect transistors connected in parallel, each of which has source and drain diffusion layers of the first conductive type.

Regarding claims 2, 5 and 6, APA teaches a gate electrode of the first field effect transistor and the source dopant diffusion region are placed over the second conductive type well that is formed on the surface of the semiconductor substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the bottom of the first conductive type well at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well in APA's device in order to prevent shorting the junction by allowing spikes to propagate longer distance.

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Regarding claim 6, APA teaches a dopant high-concentration region 20 beneath the second conductive type well, and containing second conductive type dopants with a higher dopant concentration than the second conductive type well.

***Response to Arguments***

Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B-E are cited as being related to ESD devices having N wells.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

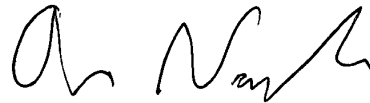
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

A handwritten signature in black ink, appearing to read 'Ori Nadav', with a stylized flourish at the end.

O.N.  
April 20, 2004

ORI NADAV  
PATENT EXAMINER  
TECHNOLOGY CENTER 2800